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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/004,536
Filing Date: October 31, 2001
Appellant(s): SINDHU ET AL.

Kent J. Sieffert
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed December 19, 2006 appealing from the Office action mailed June 16, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

NEW GROUND(S) OF REJECTION

Claims 1-9, 11-20, 22-26, 28-32, 34 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Bass et. al (USPN 6,460,120).

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US 6424658 B1	Mathur; Harish N.	7-2002
US 6246680 B1	Muller; Shimon et al.	6-2001
US 6460120 B1	Bass; Brian et al.	10-2002
US 5008878 A	Ahmadi; Hamid et al.	4-1991

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-9, 11-20, 22-26, 28-32, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mathur (USPN 6,424,658) in view of Muller et al. (USPN 6,246,680) (hereinafter Muller)

1. Referring to independent claim 1, Mathur discloses a routing component 22, 24 comprising:

a first interface (i.e. network interface) to communicate with a first network interface (Figure 3, ref. 32, 34);

a second interface (i.e. data bus 42) wherein the first interface and the second interface are integrated within a single integrated circuit (i.e. network switch chip) (Figure 3, ref. 36, 38; col. 3, lines 55-60); and

an embedded memory (i.e. FIFO) within the integrated circuit (Figure 3, ref. 32, 34);

at least one control unit that determines a direction of communication for the data between the first and second interfaces (i.e. depending on which interface the packet is received upon, this determines the direction of communication, a packet received on the first interface cannot come from the second interface) (col. 6, lines 3-15).

Mathur does not specifically disclose a memory interface to couple the integrated circuit to an external memory for buffering data communicated in a second direction from the second interface having a higher bandwidth to the first interface having a lower bandwidth, the second interface communicates data to a second routing component using a switch internal to the router, and that the control unit accesses a forwarding table . In analogous art, Muller discloses another routing component which includes a memory interface 220 to couple the element to an external memory for buffering data communicated from the second interface to the first interface (col. 4, line 61 to col. 5, line 4). Muller furthermore discloses the second interface (i.e. cascading interface 225 connects to a second routing component (i.e. switch element 100) using a switch (i.e. mesh topology) internal to the router 101 (col. 4, lines 15-40). Muller furthermore discloses the control unit (i.e. CPU 161 requests forwarding decisions from the forwarding database 113, 140 to determine a network destination for the data (i.e. receipt of a forwarding decision, forwarding the pointers to the output ports indicated by the forwarding decision) (col. 4, lines 41-60). It would have been obvious to one of ordinary skill in the art to combine the teaching of Muller with Mathur to provide a buffered architecture to Mathur to provide temporary storage for efficient allocation of

per port buffering that is proportional to the amount of traffic through a given port as supported by Muller (col. 8, lines 35-40).

2. Referring to claim 2, Mathur discloses a first control unit to buffer in the embedded memory data that is received from the first interface and forwarded to the second interface (e.g. abstract). Mathur does not disclose a second control unit to buffer in the external memory data that is received from the second interface and forwarding to the first interface. In analogous art, Muller discloses another routing component which includes a second control unit 220 to buffer in the external memory data that is received from the second interface and forwarding to the first interface (col. 7, line 35 to col. 8, line 35). It would have been obvious to one of ordinary skill in the art to combine the teaching of Muller with Mathur to provide a buffered architecture to Mathur to provide temporary storage for efficient allocation of per port buffering that is proportional to the amount of traffic through a given port as supported by Muller (col. 8, lines 35-40).

3. Referring to claim 3, Mathur in view of Muller disclose the system substantively as described in claim 2. Mathur in view of Muller do not specifically disclose the external memory has a greater storage capacity than the embedded memory, however it is well known that external memory (i.e. hard drives, flash drives, etc.) can have a higher storage capacity than embedded memory such as registers and Random Access Memory. Therefore it would have been obvious to assume the external memory would

have a greater storage capacity than the embedded memory since it would allow for more packets to be stored and thereby reducing page faults in the external device.

4. Referring to claim 4, Mathur discloses the first interface comprises a WAN (i.e. network) interface (col. 6, lines 3-15).

5. Referring to claim 5, Mathur discloses the second interface comprises a switch fabric interface (i.e. token ring) (Figure 3, ref. 30, 42).

6. Referring to claim 6, Mathur discloses the switch fabric interface communicates crossbar data (i.e. data transmitted between routing components (co. 7, lines 10-25).

7. Referring to claim 7, Mathur discloses the routing component is implemented using an ASIC (it is understood in the art and in the specification as defined on page 4, an ASIC is a circuit board or chip which is designed for a particular function, in this case the routing component 12 is integrated on a single switch chip, therefore it is implemented as an Application Specific IC, the Application in this case is to provide routing function) (Figure 2; col. 3, lines 55-60).

8. Referring to claim 8, Mathur discloses the embedded memory comprises a RAM (i.e. DRAM) (Figure 2, ref. 20).

9. Claims 9, 11-20, 22-26, 28-32, 34 and 35 are rejected for similar reasons as stated above. Furthermore Mathur discloses comprising a second router having an embedded memory to store data communicated using the second network interface (col. 6, lines 3-10).

*******NEW REJECTION********

Claims 1-9, 11-20, 22-26, 28-32, 34 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Bass et. al (USPN 6,460,120) (hereinafter Bass).

10. Referring to claim 1, Bass discloses a routing component (13-1 to 13-k and 17-1 to 17-k, however a more detailed version of the routing component can be found in Figure 1, ref. 10) of a router (i.e. switching system) (Figure 16) comprising:

a first interface (i.e. DMU BUS 13 connecting the Ethernet physical layer 38 with PMM-up multiplexed MAC's 14) to communicate data with a network (i.e. Ethernet PHY) (Figure 1);

a second interface (i.e. DASL A/B 22/24) to communicate data to a second routing component using a switch internal to the router (i.e. utilizing the DASL, the component sends data via the switching fabric 11 to the outbound routing component 17-1, via the inbound DASL A/B 26, 28) (Figure 16; col. 27, line 55 to col. 26, line 32);

an embedded memory within the integrated circuit (i.e. internal S-RAM data store 15) (Figure 1);

a memory interface to couple the integrated circuit to an external memory (i.e. connection connecting D-RAM's Data store on the Egress side) (col. 9, lines 45-67; col. 12, lines 52-67);

at least one control unit (i.e. embedded processors complex 12 including switching fabric device) that receives data from the network via the first interface and accesses a forwarding table to determine a network destination for the data (i.e. the use of a forwarding table is described in Patent no. 5,008,878 incorporated by reference, col. 7, lines 18-24: "...prestored tables for associating packet destination addresses with local routing addresses") (col. 5, lines 20-31;col. 13, lines 18-36);

wherein the control unit buffers data using the embedded memory internal to the integrated circuit when the destination requires forwarding the data through the switch internal to the router (i.e. ingress packets are stored on the internal S-RAM data store 15) (col. 11, lines 45-56);

wherein the control unit buffers data using the external memory external to integrated circuit when the destination requires forwarding the data to the network via the first interface (i.e. packets are stored in the egress/external data store) (col. 9, lines 45-67).

11. Referring to claim 2, Bass discloses the at least one control unit comprises:

a first control unit (i.e. EDS-UP enqueue dequeue scheduling 16) to buffer in the embedded memory data that is received from the first interface and is forwarded to the second interface) (col. 12, lines 30-40); and

a second control unit (i.e. EDS-DN 34) to buffer in the external memory data that is received from the second interface and is forwarded to the first interface) (col. 12, line 59).

12. Referring to claim 3, Bass discloses the external memory is of a greater capacity than the internal memory (the S-RAM embedded memory can buffer up to 2048 64-byte frames, versus the D-RAM external memory, which can store 256K 64-byte frames) (col. 9, lines 55-60; col. 10, lines 3-4).

13. Referring to claim 4, Bass discloses the first interface comprises a WAN interface (i.e. Ethernet physical interface) (Figure 1, ref. 38; col. 6, line 59 to col. 7, line 23).

14. Referring to claim 5, Bass discloses the second interface comprises a switch interface (Figure 16, ref. 13-1).

15. Referring to claim 6, Bass discloses the switch interface communicates crossbar data (i.e. the switching fabric connects the input port to all output ports) (Figure 16; col. 27, line 65 to col. 28, line 7).

16. Referring to claim 7, Bass discloses the component is an ASIC (col. 3, lines 20-25).

17. Referring to claim 8, Bass discloses the memory is RAM (i.e. D-RAM) (Figure 1).

18. Claim 9, 11-20, 22-26, 28-32, 34 and 35 are rejected for similar reasons as stated above. Furthermore Bass discloses a plurality of the ports found in Figure 1 in Figure 16, ref. 13-1 to 13-k and 17-1 to 17-k) and therefore discloses at least a second routing component with embedded data.

(10) Response to Argument

Appellant's arguments found in the Brief (pages 12-18 have been fully considered but are not persusive.

In the remarks, Appellant argues, in substance, that (1) the combination of Mathur and Muller fail to disclose the use of buffering packets differently based on the destination specified within the packet and the bandwidth differences between the interfaces.

As to point (1) Appellant is incorrect. As a preliminary manner, the Examiner would like to point out that the amendment dealing with the bandwidths of the respective

interfaces (i.e. the network versus the switching fabric) was removed in the previous amendment. Appellants should be aware that Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). As such the consideration of bandwidth plays no part in the rejection. Furthermore Appellant is attempting to refute the rejection by attacking each of the references individually. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The rejection is based upon a combination of the references Mathur and Muller. Sufficient motivation has been provided which would find it obvious to combine the references to meet the claimed invention. By this rationale, the rejection is maintained.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

This examiner's answer contains a new ground of rejection set forth in section **(9)** above. Accordingly, appellant must within **TWO MONTHS** from the date of this answer

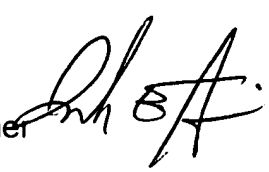
exercise one of the following two options to avoid *sua sponte* **dismissal of the appeal** as to the claims subject to the new ground of rejection:

(1) **Reopen prosecution.** Request that prosecution be reopened before the primary examiner by filing a reply under 37 CFR 1.111 with or without amendment, affidavit or other evidence. Any amendment, affidavit or other evidence must be relevant to the new grounds of rejection. A request that complies with 37 CFR 41.39(b)(1) will be entered and considered. Any request that prosecution be reopened will be treated as a request to withdraw the appeal.

(2) **Maintain appeal.** Request that the appeal be maintained by filing a reply brief as set forth in 37 CFR 41.41. Such a reply brief must address each new ground of rejection as set forth in 37 CFR 41.37(c)(1)(vii) and should be in compliance with the other requirements of 37 CFR 41.37(c). If a reply brief filed pursuant to 37 CFR 41.39(b)(2) is accompanied by any amendment, affidavit or other evidence, it shall be treated as a request that prosecution be reopened before the primary examiner under 37 CFR 41.39(b)(1).

Extensions of time under 37 CFR 1.136(a) are not applicable to the TWO MONTH time period set forth above. See 37 CFR 1.136(b) for extensions of time to reply for patent applications and 37 CFR 1.550(c) for extensions of time to reply for ex parte reexamination proceedings.

Respectfully submitted,

Joseph E. Avellino, Examiner 

A Technology Center Director or designee must personally approve the new ground(s) of rejection set forth in section (9) above by signing below:

Approved

PAUL SEWELL
ACTING DIRECTOR

Conferees:

DAVID WILEY
SUPERVISORY PATENT EXAMINER
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